Knight Foundation School of Computing and Information Sciences

Course Title: Structured Computer Organization

Date: 2/12/2018

Course Number: CDA 4101

Number of Credits: 3

| Subject Area: Computer Organization | Subject Area Coordinator: | |
|---|--|--|
| | Dong Chen | |
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| Catalog Description: Covers the levels of o | rganization in a computer: Design of | |
| memory, buses, ALU, CPU; design of micro | program. Covers virtual memory, I/O, | |
| multiple processes, CISC, RISC and parallel | architectures. | |
| Textbook: Structured Computer Organization | on, 6 th Edition, Andrew S. Tanenbaum | |
| Prentice Hall (ISBN: 0-13-291652-5) | | |
| References: Computer Organization and Design: The Hardware/Software Interface, | | |
| 3 rd Edition | | |
| David A. Patterson, John L. Hennessy | | |
| Morgan Kaufmann (ISBN: 0123706068) | | |
| Prerequisites Courses: CDA 3103, COP 3337 and MAD 2104 or COT 3100 | | |
| | | |
| Corequisites Courses: None | | |

Type: Required for CS Major

Prerequisites Topics:

- Digital logic and Boolean algebra
- Machine level representation of data
- Assembly level machine organization
- Fundamental data structures

Course Outcomes:

- 1. Master the design of advanced combinational circuits
- 2. Master the design of memory and the ALU.
- 3. Master control unit design and RISC architectures
- 4. Be familiar with cache architectures, branch predictions, scheduling of multiple instruction issue and flow control
- 5. Be exposed to parallel architectures, including configurations, shared-memory, message passing, and taxonomy.

Relationship between Course Outcomes and Program Outcomes

| BS in CS: Program Outcomes | Course Outcomes |
|--|-----------------|
| a) Demonstrate proficiency in the foundation areas of Computer Science including mathematics, discrete structures, logic and the theory of algorithms | 1 |
| b) Demonstrate proficiency in various areas of Computer Science including data structures and algorithms, concepts of programming languages and computer systems. | 1, 2, 3, 4, 5 |
| c) Demonstrate proficiency in problem solving and application of software engineering techniques | 1 |
| d) Demonstrate mastery of at least one modern programming language and proficiency in at least one other. | |
| e) Demonstrate understanding of the social and ethical concerns of the practicing computer scientist. | |
| f) Demonstrate the ability to work cooperatively in teams. | |
| g) Demonstrate effective communication skills. | |

Assessment Plan for the Course & how Data in the Course are used to assess Program Outcomes

Student and Instructor Course Outcome Surveys are administered at the conclusion of each offering, and are evaluated as described in the School's Assessment Plan: https://abet.cs.fiu.edu/csassessment/

Outline

| Outime | | | | |
|--------|---------------------------------------|----------------------|---------|--|
| | Торіс | Number of | Outcome | |
| | | Lecture Hours | | |
| Intro | oduction to architecture | 6 | 1,3,4 | |
| 0 | Hierarchy of virtual machines | | | |
| 0 | von Neumann architecture | | | |
| 0 | CPU instruction execution cycle | | | |
| 0 | Overview of parallel architectures | | | |
| 0 | I/O devices, RAID | | | |
| 0 | Review of basic logic circuit design | | | |
| Digi | tal logic: Design of | 14 | 1,3 | |
| 0 | Multiplexer, demultiplexer, encoder, | | | |
| | decoder | | | |
| 0 | Arithmetic Logic Unit, Shifter | | | |
| 0 | Latch, flip-flop, register, memory | | | |
| | organization | | | |
| 0 | Bus protocols, arbitration, DMA | | | |
| 0 | Data path, control unit | | | |
| 0 | Microprogram | | | |
| • Perf | ormance enhancement | 9 | 2 | |
| 0 | Instruction prefetch | | | |
| 0 | Pipelining, pipeline hazards | | | |
| 0 | Cache architecture | | | |
| 0 | Branch prediction | | | |
| 0 | Dynamic scheduling of instructions | | | |
| 0 | Speculative execution | 7 | 2.4 | |
| | ruction set architecture | 7 | 3,4 | |
| 0 | CISC vs RISC | | | |
| 0 | RISC Register file | | | |
| 0 | Expanding opcode | | | |
| 0 | Stack addressing mode Flow control | | | |
| 0 | | 3 | 15 | |
| | anced architecture | 3 | 4,5 | |
| 0 | Taxonomy of parallel architectures | | | |
| 0 | Exposure to shared memory | | | |

Course Outcomes Emphasized in Laboratory Projects / Assignments

| | Outcome | Number of Weeks |
|---|-----------------------------|-----------------|
| 1 | Microprogram design | 3 |
| | Outcomes: 1,3 | |
| 2 | Complex microprogram design | 3 |
| | Outcomes: 1,3 | |

Oral and Written Communication

No significant coverage

| Written Reports | | Oral Pres | sentations |
|-----------------|----------------|-----------|------------------|
| Number | Approx. Number | Number | Approx. Time for |
| Required | of pages | Required | each |
| 0 | 0 | 0 | 0 |

Social and Ethical Implications of Computing Topics

No significant coverage

| Торіс | Class time | student performance measures | |
|-------|------------|------------------------------|--|
| | | | |

Approximate number of credit hours devoted to fundamental CS topics

| Fundamental CS Area | Core Hours | Advanced Hours |
|---------------------------|-------------------|----------------|
| Algorithms: | | |
| | | |
| Software Design: | | |
| Computer Organization and | | |
| Architecture: | 3.0 | |
| Data Structures: | | |
| | | |
| Concepts of Programming | | |
| Languages | | |

Theoretical Contents

| Topic Class time | | |
|--------------------------|-----|--|
| Boolean algebra | 1.0 | |

Problem Analysis Experiences

1. Instruction set analysis

Solution Design Experiences

- 1. Digital circuit design
- 2. Microprogram design

The Coverage of Knowledge Units within Computer Science Body of Knowledge¹

| Knowledge Unit | Торіс | Lecture Hours |
|----------------|---|----------------------|
| <u>AR4</u> | Storage systems, coding, data integrity, | 6 |
| | memory organization, latency, cycle time, | |
| | cache memories | |
| <u>AR5</u> | I/O fundamentals, external storage, RAID | 6 |
| | architectures, bus protocols, bus arbitration, | |
| | DMA | |
| <u>AR6</u> | Implementation of simple datapath, control | 14 |
| | unit, pipelining, instruction level parallelism | |
| <u>AR7</u> | SIMD, MIMD, VLIW, interconnection | 5 |
| | networks, shared memory systems, cache | |
| | coherence | |
| <u>AR8</u> | Superscalar, superpipe lining, branch | 8 |
| | prediction, prefetching, speculative execution, | |
| | multiple instruction issue | |

¹See <u>https://www.acm.org/binaries/content/assets/education/cs2013_web_final.pdf</u> for a description of Computer Science Knowledge units